Computer Maintenance

Unit Subtitle: Bus Structures

Excerpted from www.howstuffworks.com

Objectives

- Define bus structures
- Identify the ISA bus
- Interpret the bus schematic for a computer
- Identify the PCI bus
- Differentiate between the different bus structures
- Learn what the future holds for bus structures

2

Bus Structures

- There are a lot of incredibly complex components in a computer.

- All of these parts need to communicate with each other.

- Communication needs to be fast and efficient.

- That's where the **bus** comes in.

- A bus is the channel or path between the components in a computer.

3

Bus Structures (Continued)

- Buses have evolved over the years to match the performance of all other computer components.

- The evolution of the bus has been slow compared to other technologies.

- Most computers sold today still have an **Industry Standard Architecture** (ISA) bus that will accept computer cards developed for the original IBM PC in the early 1980s.

4

Typical Bus Structures

- A typical computer has two key buses.
- **The system bus** or **local bus**
  - Connects the microprocessor (central processing unit) and the system memory
- Other buses – ISA and PCI
  - Connect to the system bus via the **bridge**
  - The bridge is part of the computer's chipset and acts as a traffic cop, integrating the data from the other buses to the system bus.

Typical Bus Structures (Cont.)
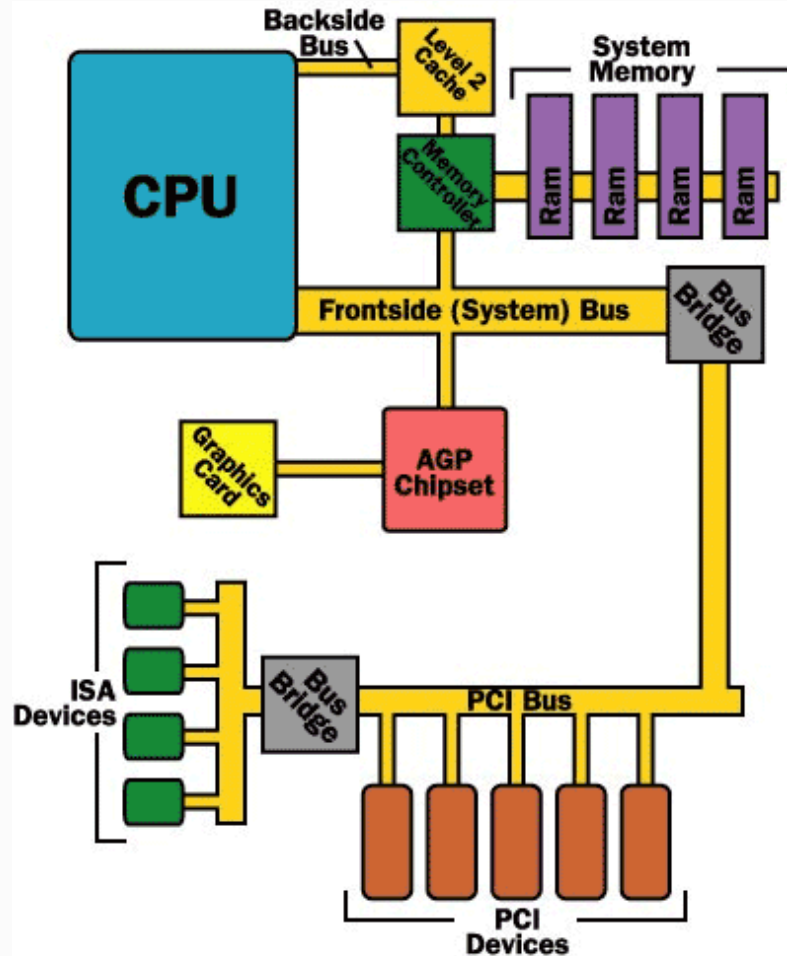
©2001 HowStuffWorks

This illustration shows how the various buses connect to the CPU.

PCI Bus

- Intel introduced a new bus standard in early 1990s.
- **Peripheral Component Interconnect (PCI)**
- PCI presents a hybrid between ISA and VL-Bus.
- It provides direct access to system memory for connected devices.
- It uses a bridge to connect to the front side bus, and therefore to the CPU.
- It is capable of even higher performance than VL-Bus, while eliminating the potential for interference with the CPU.

PCI Bus Cont.

- Can connect up to five external components

- You can have more than one PCI bus on the same computer.

- The PCI bridge chip regulates the speed of the PCI bus independently of the CPU's speed.

- This provides higher reliability and ensures that PCI hardware manufacturers know exactly what to design for.

@2001 HowStuffWorks

Typical Bus Structures (Cont.)

The other main bus, the **shared bus**, is for connecting additional components to the computer. It is called a shared bus because it lets multiple devices access the same path to the CPU and system memory. These devices includes such items as:

Modem   Hard drive
Sound card   Graphics card
Controller card   Scanner

Typical Bus Structures (Cont.)

- As technology advanced, other buses were developed.
- **Extended Industry Standard Architecture** (EISA)
  - 32 bits at 8 MHz
- **Vesa Local Bus** (VL-Bus).
  - 32 bits wide and operated at the speed of the local bus – normally the speed of the processor itself.

Bus Types

Bus Type	Bus Width	Bus Speed	MB/sec
ISA	16 bits	8 MHz	16 MBps
EISA	32 bits	8 MHz	32 MBps
VL-bus	32 bits	25 MHz	100 MBps
VL-bus	32 bits	33 MHz	132 MBps
PCI	32 bits	33 MHz	132 MBps
PCI	64 bits	33 MHz	264 MBps
PCI	64 bits	66 MHz	512 MBps
PCI	64 bits	133 MHz	1 GBps

The Future

- As processor speeds steadily climb into the GHz range, companies are working to develop a next-generation bus standard.

- Many feel that PCI, like ISA before it, is fast approaching the upper limit of what it can do.

- They propose doing away with the shared-bus technology used in PCI and moving to a **point-to-point switching connection**.

- This means that a direct connection between two devices (nodes) on the bus is established while they are communicating with each other.

- By providing multiple direct links such a bus can allow several devices to communicate with no chance of slowing each other down.

The Future (Continued)

@2001 HowStuffWorks

- **HyperTransport** – a standard proposed by Advanced Micro Devices, Inc. (AMD)
- Designed specifically for connecting internal computer components to each other, but not for connecting external devices such as removable drives.

The Future (Continued)

- Intel has announced **3GIO** (Third Generation I/O), a proposed standard that industry experts believe will compete with HyperTransport to replace PCI. Intel's plans for 3GIO include:
  - Speeds in excess of 10 GHz
  - Full serial I/O architecture
  - Point-to-point connections
  - Low pin count

The Future (Continued)

- 3GIO is still in the preliminary stages of specification.

- Has a way to go before it can be considered a standard

- 3GIO, HyperTransport, and Infiniband, want to move away from the bus-based system toward a direct-connection system.

- Even so, ISA is still in use, and PCI is expected to hang around for a long time yet.